A FLIP-CHIP MMIC DESIGN WITH CPW TECHNOLOGY IN THE W-BAND

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ABSTRACT

We designed and fabricated a W-band flip-chip MMIC amplifier with a coplanar wave-guide (CPW) transmission line using 0.15 μm InGaP/InGaAs HEMT technology. In addition, we present a test structure for obtaining an accurate flip-chip CPW line model, and demonstrate a two-stage flip-chip MMIC amplifier with a gain of 12 dB at 79 GHz to validate this model.

1. INTRODUCTION

Flip-chip bonding (FCB) is one of the attractive technologies for reducing fabrication costs and assembly costs, and for improving the performance of MMICs in W-band applications such as automotive radar systems and multi-gigabit fiber-optic communication systems. Many applications which use the FCB technology have been researched, and many have exhibited the requirements and qualities needed for low-cost mm-wave application[1]. A FCB technology using Au/AuSn micro-pillars that are 20 μm tall and 40 μm in diameter has been developed, and its mechanical and thermal reliability in mm-wave applications has been reported on [2]. Coplanar wave-guide (CPW) transmission line technology must be used in order to develop low-cost flip-chip MMICs with the FCB technology since there is no wafer thinning process, no via etch, and no backside processing of the wafer. Therefore, applying the CPW line to the development of flip-chip MMICs is very advantageous for realizing low-cost millimeter-wave applications[3].

Accurate flip-chip CPW line models are needed in order to design flip-chip MMICs using a CPW line for the W-band application. An actual flip-chip CPW line contains signal transition parts such as pillars or bumps to transmit a signal from external feed line to the CPW line. When characterizing the actual CPW lines, however, the signal transition part is an obstacle in the de-embedding of the external feed lines since the transverse electromagnetic field expands toward each line. In order to characterize the flip-chip CPW lines accurately, we developed a test structure which gives the same environment of the actual flip-chip CPW line without a signal transition pillar. In this paper, we report on the modeling of a flip-chip CPW transmission line using the test structure and the validation of the design accuracy of the model. This is done by designing a flip-chip MMIC two-stage amplifier with a 0.15 μm InGaP/InGaAs HEMT in the W-band.

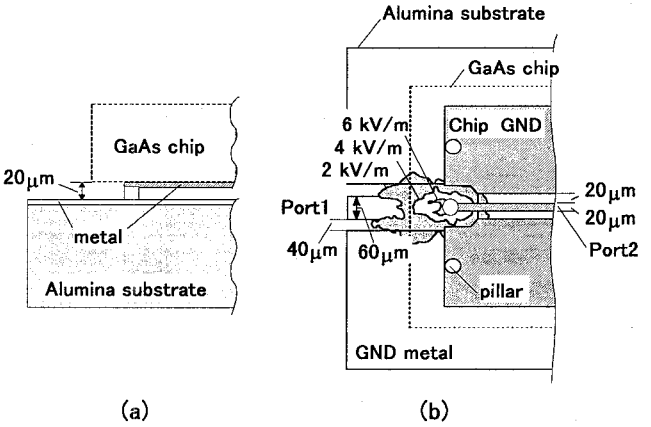

Fig. 1. Electromagnetic field simulation for an actual flip-chip coplanar wave-guide. (a) The side view of analyzed structure. (b) Top view of the electromagnetic field distribution around signal transition pillar at 76 GHz.

2. ELECTROMAGNETIC FIELD ANALYSIS OF THE FLIP-CHIP

Figures 1 (a) and (b) show a portion of an actual flip-chip structure, which includes a signal transition pillar. Figure 1 also shows a simulated result of a magnitude contour map of the electric field distribution at a distance of 10 μm from the alumina substrate at 76 GHz. The simulation was performed using a 3-dimensional full wave electromagnetic field simulator (Ansoft Eminence). In this simulation, an electromagnetic source was connected at port 1. As seen in Figure1(b), the electric field expands under the CPW line on the GaAs chip. This leads to an interaction between the signal transition pillar and CPW line, and makes it difficult to determine the reference plane in de-embedding each line. Therefore, we propose a test structure and an experimental technique to model the flip-chip CPW lines without signal transition pillars.

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3. THE TEST STRUCTURE

The test structure consists of two parts. One is a CPW line fabricated on a GaAs substrate with a thickness of 600 μm. Here, 2.0 μm thick gold (Au) metal is used for the CPW line. The other part is a chip, the whole surface is coated by Au metal. It is used as a ground lid for the CPW line and positioned above it (Figure 2). The lid chip is mounted by a flip-chip bonding tool of which a precise positioning is guaranteed on micro pillars fabricated on the CPW line ground metal so that the metallized surface faces the CPW line[2]. The pillar height, diameter and minimum distance between pillars are 20 μm, 40 μm, and 125 μm, respectively. Figure 3 shows a microphotograph of the structure and the corresponding CPW lines. As seen in Figure 3 (b), there are three parts of the CPW lines in the structure, the face-up feed line, the line that lies underneath the lid chip surface, and the line under metal. To minimize electrical discontinuity at the interface between the face-up part and the ground-face part, the line widths of the parts which are face-up was optimized to be 50 ohms. The S-parameters of the CPW lines were measured using a vector network analyzer (VNA) with coplanar ground-signal-ground micro probes from 0.45 GHz to 110 GHz. The transmission line parameters were extracted during measurements. Figure 4 shows the extracted and simulated the transmission line parameters of the CPW through-line of the test structure after de-embedding the feed lines and the lines which are underneath the lid chip. The simulation was performed with the moment method using the Gelerkin technique[4]. Assuming $RG << \omega^2 LC$ in the actual characteristic impedance ($Z = \sqrt{(R + j\omega L)/(G + j\omega C)}$), we used following equations.

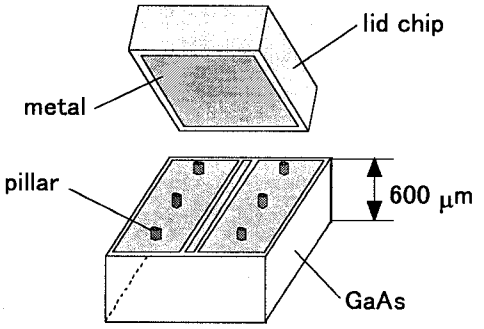
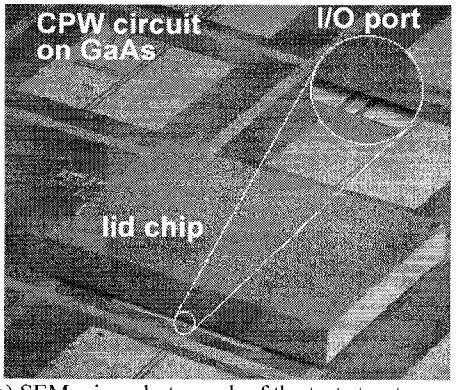
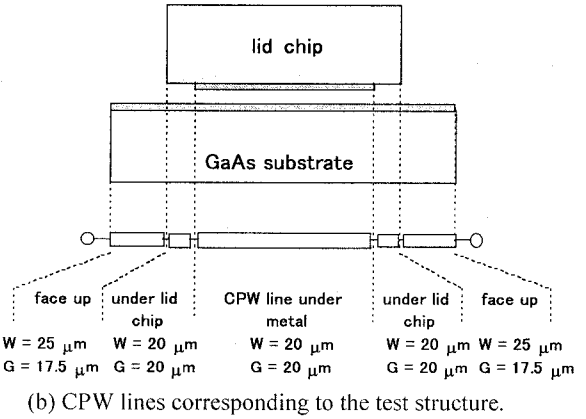


Fig. 2. A schematic of the test structure. The metal surface of the lid chip faces to the CPW line.



(a) SEM microphotograph of the test structure.



(b) CPW lines corresponding to the test structure.

Fig. 3. The test structure. (a) SEM microphotograph. (b) CPW lines corresponding to the test structure.

$$Z_0 = \sqrt{\frac{L}{C}} \quad (\Omega) \quad (1)$$

$$E_{eeff} = L \cdot C \cdot c_0^{\,2} \quad (2)$$

$$A_{ttn} = \frac{R}{2 \cdot Zo \cdot 0.1156} \cdot \sqrt{\frac{F_C}{f_0}} \quad (\mathrm{dB/m}) \quad (3)$$

$$tan\delta = \frac{G}{2\pi \cdot f_0 \cdot C} \quad (4)$$

Here, Z_0 is the loss less characteristic impedance, E_{eff} is the effective dielectric constant, A_{ttn} the conductor loss of the line, and tanδ a dielectric loss tangent. L, C, R and G are the inductance, capacitance, resistance and conductance per unit length of the transmission line, respectively. F_C and f_0 are reference and focused frequency respectively. c_0 is the velocity of light. De-embedding was carried out with an ABCD matrix manipulation. We obtained Z_0=49.0 ohms, an E_{eff}=5.41 and an A_{ttn}=300 dB/m from measured data for the line widths of 20 μm, ground to ground spacing of 60 μm and pillar height of 20 μm. We also obtained a Z_0=55.9 ohms, E_{eff}=6.33 and A_{ttn}=241 dB/m with the same line widths and ground-to ground spacing for the line without the lid chip. As mentioned in [5-7], the CPW line and the ground on the substrate interact. These results are closely agree with simulation results and indicate that W-band flip-chip MMICs which use a CPW line can be designed using the quasi-TEM mode approximation. In addition, the

test structure proposed here is advantageous in that it makes on-wafer measurements feasible. We measured various type of CPW lines such as T-junction, Cross-junction, bend

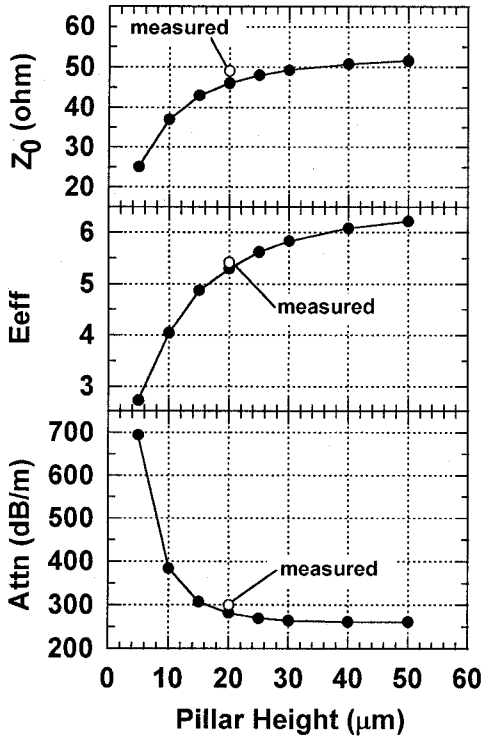


Fig. 4. Simulated and extracted transmission line parameters of the CPW line with the test structure. The line width and gaps are 20 μm respectively.

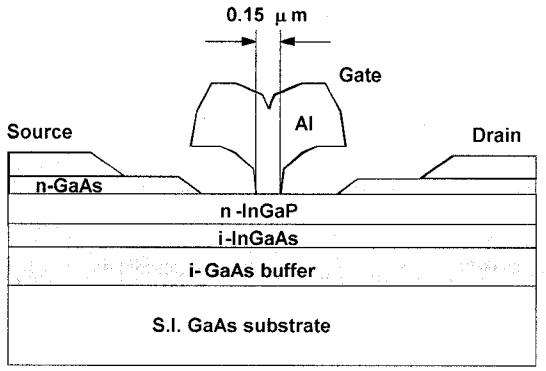


Fig. 5. Schematic cross section of 0.15 μm InGaP/InGaAs HEMT.

and so on using the test structure and extracted the transmission line parameters. We also added the model into the HP-EEsof Libra circuit simulator.

4. FLIP-CHIP CPW MMIC DESIGN AND FABRICATION

To verify the accuracy of the CPW line model using the test structure, we designed and fabricated a flip-chip

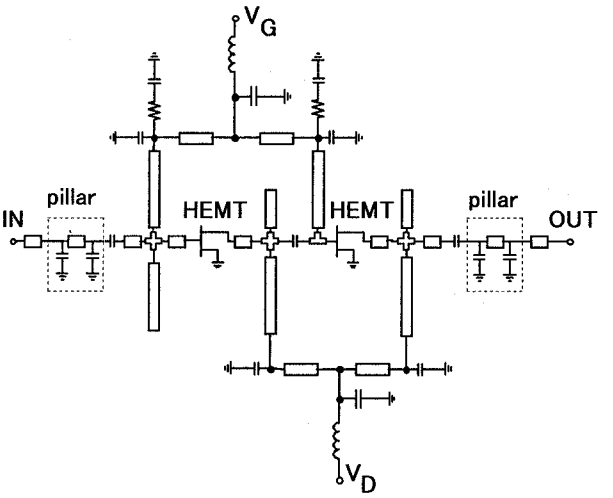


Fig. 6. Schematic diagram of flip-chip MMIC a two-stage amplifier.

MMIC two-stage amplifier with a CPW line for the W-band. For the circuit design, we employed a 0.15 μm InGaP/InGaAs HEMT using electron-beam lithography (EB) on a semi-insulated GaAs substrate. It offers a cutoff frequency (f_T) of 90 GHz and a maximum oscillation frequency (f_{max}) of 170 GHz. A schematic cross-section of the InGaP/InGaAs HEMT is shown in Figure 5. The designed amplifier employs a two-stage configuration with 80 μm wide gate HEMTs, and is designed using small signal design. The small signal S-parameters of the HEMT were measured under the same test structure described above. Open circuited stubs are used for the input, output, and inter-stage matching circuits. Figure 6 shows the schematic diagram of the two-stage amplifier. The characteristic impedance and effective dielectric constant of the signal transition pillars were roughly estimated using 3-dimensional, electromagnetic field simulator[8] and analytical method. The characteristic impedance and

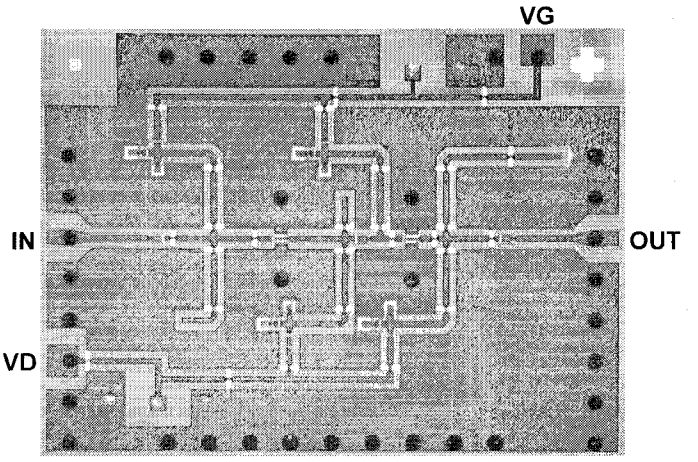


Fig. 7. A two-stage amplifier. The chip size is 1.9 x 1.25 mm^2.

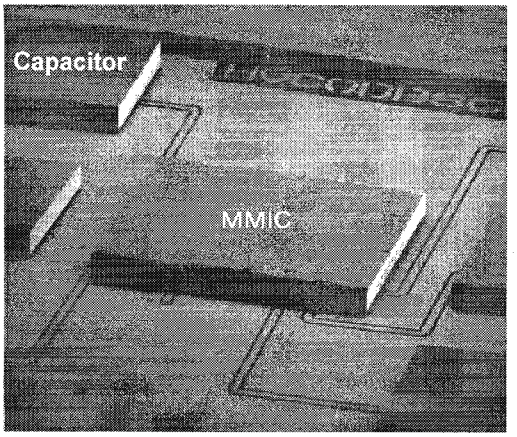


Fig. 8. SEM microphotograph of the flip-chip MMIC.

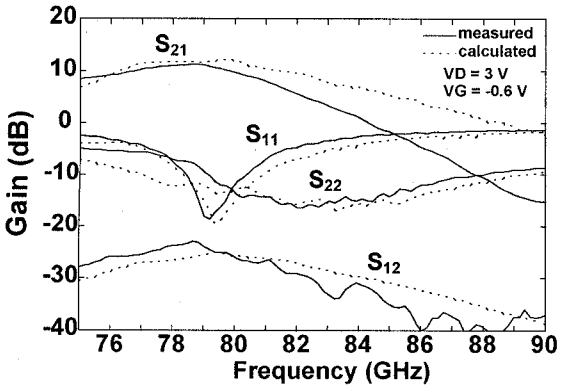


Fig. 9. Measured and simulated S-parameters of the flip-chip InGaP/InGaAs HEMT MMIC two-stage amplifier.

dielectric constant of the pillar are estimated to be 207 ohms and 1 respectively. As mentioned previously, these values, however are not accurate, but in this case, the effects on the total characteristics of the MMIC performances are negligible small [5,6]. Figure 7 shows a microphotograph of the MMIC amplifier chip. The chip size was 1.9 x 1.25 mm^2. The MMIC chip was mounted on an alumina substrate with patterned DC bias lines and RF feed lines on its surface. Figure 8 shows a SEM microphotograph of the flip-chip mounted MMIC amplifier with capacitors to eliminate unexpected oscillation in the low frequency range. The flip-chip MMIC amplifier was tested using the VNA from 75 GHz to 110 GHz. Figure 9 shows the measured S-parameters of the biased flip-chip MMIC amplifier with 3V for the drain and -0.6 V for the gate. The obtained forward gain (S_{21}) and isolation (S_{12}) are 12 dB and -27 dB at 79 GHz respectively. The input return loss (S_{11}) and output return loss (S_{22}) are -20 dB and -10 dB respectively.

5. CONCLUSION

We proposed a test structure to model a flip-chip CPW transmission line for W-band applications. We applied the model to the design of a 0.15 μm flip-chip InGaP/InGaAs HEMT MMIC two-stage amplifier in the W-band. The good agreement of the calculated S-parameters with the measured data suggests that the flip-chip CPW line model demonstrated here is completely accurate. This flip-chip CPW modeling technique is essential for designing flip-chip mounted MMIC applications in the W-band.

ACKNOWLEDGEMENT

The authors would like to thank M. Takikawa, N. Okubo and T. Yokoyama for their encouragement. We also thank M. Nishi and H. Someta for fabricating the test structure and T. Shimura for his helpful discussions on the MMIC design.

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